Customer Training Workshop
Traveo™ II Reset System

Q4 2020

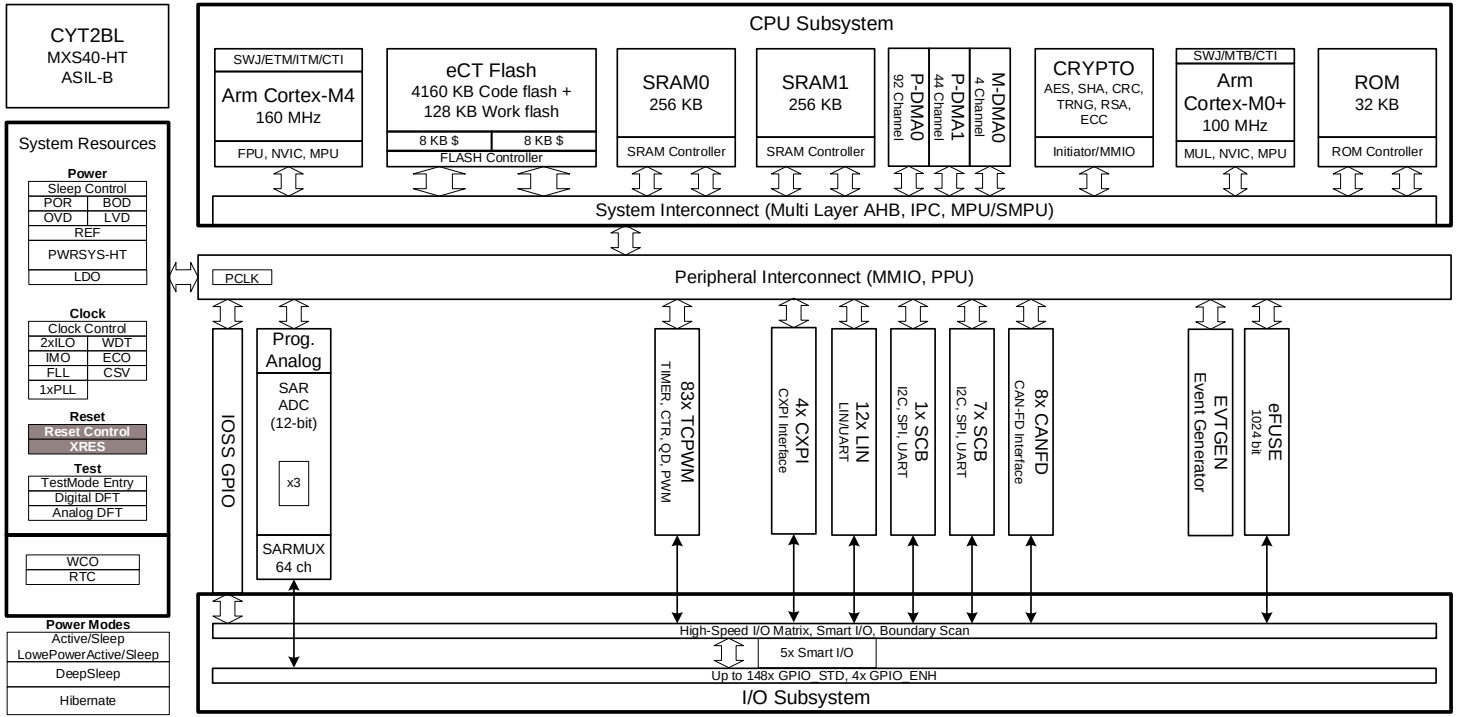
Target Products

› Target product list for this training material

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Body Controller Entry	CYT2B6	Up to 576 KB
Traveo II Automotive Body Controller Entry	CYT2B7	Up to 1088 KB
Traveo II Automotive Body Controller Entry	CYT2B9	Up to 2112 KB
Traveo II Automotive Body Controller Entry	CYT2BL	Up to 4160 KB
Traveo II Automotive Body Controller High	CYT3BB/CYT4BB	Up to 4160 KB
Traveo II Automotive Body Controller High	CYT4BF	Up to 8384 KB
Traveo II Automotive Cluster	CYT3DL	Up to 4160 KB
Traveo II Automotive Cluster	CYT4DN	Up to 6336 KB

Introduction to Traveo II Body Controller Entry

The Reset system is part of System Resources

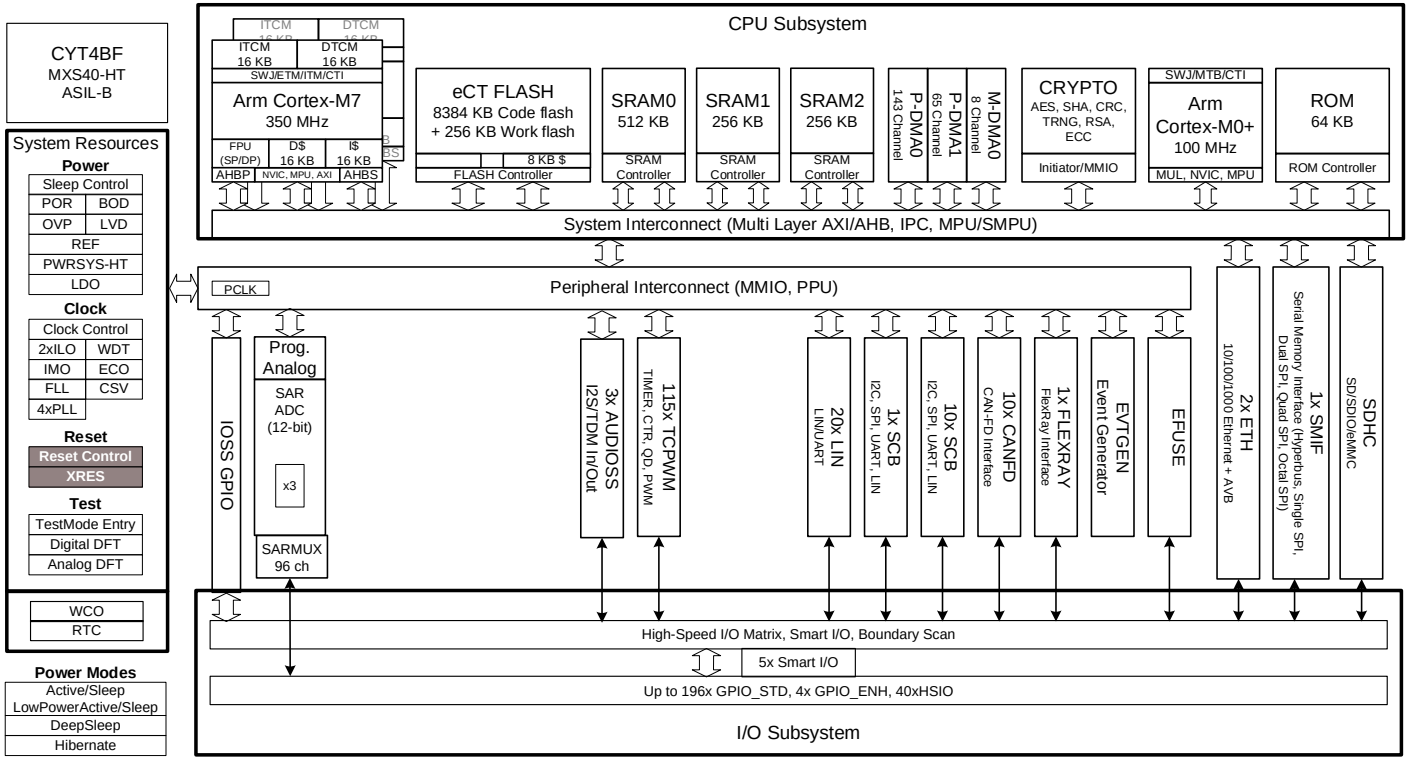


Hint Bar

Review TRM chapter 19 for additional details

Introduction to Traveo II Body Controller High

The Reset system is part of System Resources

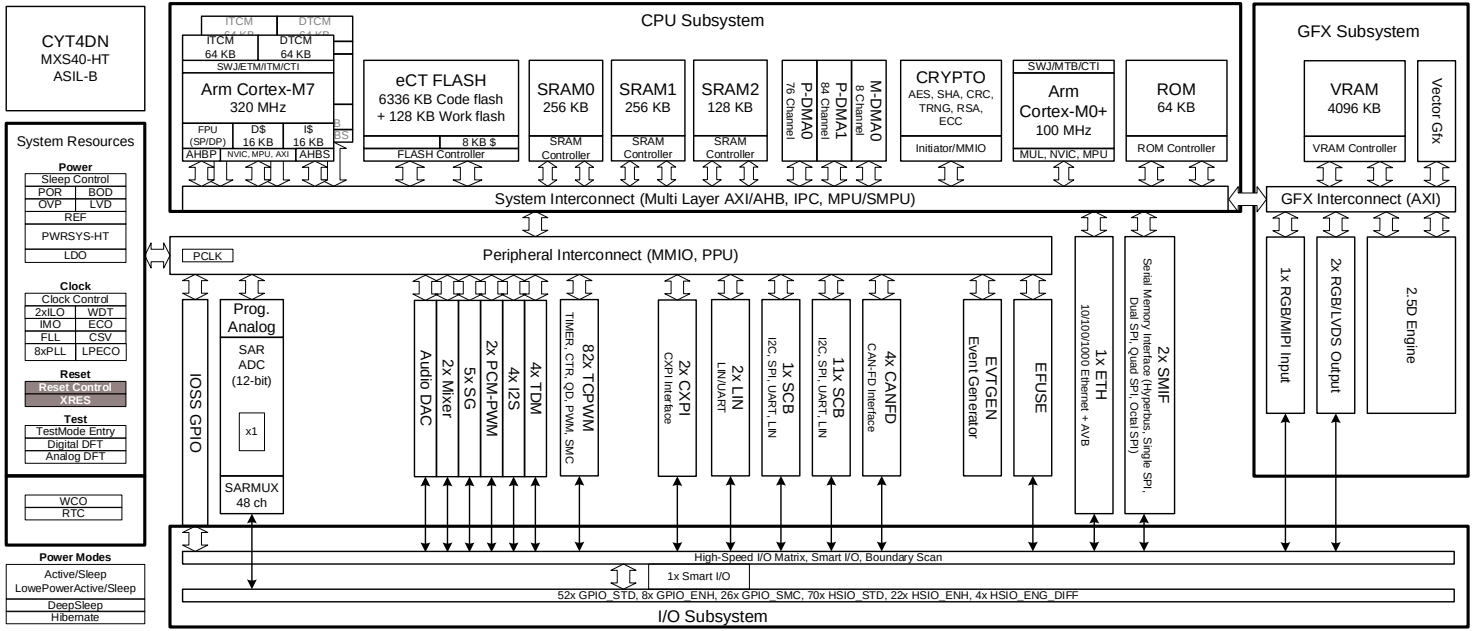


Hint Bar

Review TRM chapter 19 for additional details

Introduction to Traveo II Cluster

› The Reset system is part of System Resources



Hint Bar

Review TRM chapter 19 for additional details

Reset System Overview

- Traveo II supports several types of resets that guarantee error-free operation during power-up and allow the device to reset based on user-supplied external hardware or internal software reset signals
- Resets are asserted (triggered) asynchronously and deasserted (released) synchronously on a positive edge of the related clock
- Reset sources:
  - POR[1], BOD[2], OVD[3], OCD[4]
  - External reset (XRES_L)
  - WDT[5], MCWDT[6]
  - Hibernate wakeup reset
  - Internal system reset
  - Fault
  - CSV[7]

Hint Bar

Review the Power Supply and Monitoring training section for additional POR, BOD, OVD, and OCD details

Review the Watchdog Timer training section for additional WDT and MCWDT details

Review the Device Power Mode training section for additional Hibernate details

Review the Fault Subsystem training section for additional Fault details

Review the Clock System training section for additional CSV details

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[1] Power-on reset
[2] Brownout detection
[3] Overvoltage protection
[4] Overcurrent protection
[5] Watchdog timer
[6] Multi-counter watchdog timer
[7] Clock supervision

Reset Sources

Reset Source	Description
POR	POR holds the device in reset until the supply voltage VDDD reaches a sufficient level to initialize the startup circuits
BOD	BOD generates a reset if VDDD or VDDA or VCCD fall below their voltage threshold
OVD	OVD generates a reset if VDDD or VDDA or VCCD rise above their voltage threshold
OCD	OCD generates a reset if the load current of a regulator is over the regulator limit
XRES_L	XRES_L is a reset triggered by an external reset pin
WDT	WDT reset causes a reset if WDT is not serviced by the software within a specified time limit or it is serviced too early in window mode
Hibernate Wakeup Reset	Hibernate wakeup reset occurs when a wakeup source triggers an exit from Hibernate mode
MCWDT	MCWDT reset causes a reset if MCWDTs are not serviced by the software within a specified time limit or they are serviced too early in window mode
Internal system reset (Software reset)	The internal system reset is a mechanism that allows software running on any of the CPUs or a connected debugger to request a system reset
Fault Detection Reset	Fault detection reset is generated if certain faults occur
CSV	CSV initiates a reset when a monitored clock stops or is outside the configured relationship to a reference clock
Test Controller or Debugger Reset	Test controller or debugger asserted reset only resets the debug domain

Hint Bar

Review the Power Supply and Monitoring training section for additional POR, BOD, OVD, and OCD details

Review the Watchdog Timer training section for additional WDT and MCWDT details

Review the Device Power Mode training section for additional Hibernate details

Review the Fault Subsystem training section for additional Fault details

Review the Clock System training section for additional CSV details

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Reset Types and Cause Bits

Reset Type	Reset Source	Reset Cause Register [bit][1]	Clearing Source of Reset Cause Register	Block or Not Block Recording of Other Reset Causes	Available Power Mode
High-Voltage (HV)	POR	SRSS_RES_CAUSE [30]	Software	Not block recording of other HV causes	All power modes
	BOD	SRSS_RES_CAUSE [19:17]	Software or POR	Block recording of other HV causes except POR	All power modes except Hibernate mode
	OVD	SRSS_RES_CAUSE [22:20]			
	OCD	SRSS_RES_CAUSE [24:23]			
	XRES_L	SRSS_RES_CAUSE [16]			All power modes
	WDT	SRSS_RES_CAUSE [0]			All power modes
	Hibernate Wakeup Reset	PWR_HIBERNATE [7:0] PWR_HIB_DATA [31:0][2]	Software or POR or XRES	Not block recording of other causes	Hibernate mode
Low-Voltage (LV)	MCWDT	SRSS_RES_CAUSE [8:5]	Software or HV resets	Not block recording of other causes	All power modes except Hibernate mode
	Software Reset	SRSS_RES_CAUSE [4]			Active mode
	Fault Detection Reset	SRSS_RES_CAUSE [2:1]			All power modes except Hibernate mode
	CSV	SRSS_RES_CAUSE2 [16:0]			
	Test Controller or Debugger Reset	SRSS_RES_CAUSE [3]			

Hint Bar

Review the Power Supply and Monitoring training section for additional POR, BOD, OVD, and OCD details

Review the Watchdog Timer training section for additional WDT and MCWDT details

Review the Device Power Mode training section for additional Hibernate details

Review the Fault Subsystem training section for additional Fault details

Review the Clock System training section for additional CSV details

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Reset Distribution

› Mapping of reset sources to the corresponding destinations that are affected by a reset event

Reset Type	Reset Source	HV Reset Causes in RES_CAUSE	LV Reset Causes in RES_CAUSE	Data Registers in Fault	Debug Unit	Hibernate Registers	RTC	CPUs	SRAM Retention
High-Voltage (HV)	POR	X	X	X	X	X	X	X	No
	BOD		X	X	X	X		X	No
	OVD		X	X	X	X		X	No
	OCD		X	X	X	X		X	No
	XRES_L		X	X	X	X		X	No
	WDT		X	X	X	X		X	Yes[6]
	Hibernate Wakeup Reset		X	X	X			X	No
Low-Voltage (LV)	MCWDT				X[1]			X	Yes[2]
	Software reset							X	Yes[2]
	Fault Detection Reset				X[1]			X	Yes[2]
	CSV_HF[4]							X	Yes[3]
	CSV_REF[5]							X	No

Hint Bar

Review TRM section 19.1 for additional details

[1] Reset occurs if the source triggers during DeepSleep
[2] Yes, if orderly shutdown of the RAM is done
[3] Yes, if orderly shutdown of the RAM is done and the CSV resets are not from CSV_HF0
[4] Clock supervision for High-Frequency Clock
[5] Clock supervision for Reference Clock
[6] Yes, if orderly shutdown of the RAM is done only during a warning interrupt

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Revision History

Revision	ECN	Submission Date	Description of Change
**	6129736	04/10/2018	Initial release
*A	6329104	10/02/2018	Added pages 2, 4, 5, 8, 9, and the note descriptions for all pages Updated pages 3 and 7
*B	6592032	06/05/2019	Changed XRES to XRES_L. Updated page 2, 3, 4, 8. Added page 5.
*C	7008763	10/21/2020	Updated page 2, 3, 7, 8, 9.
*D	7044287	12/9/2020	Updated page 7, 8, 9.