Customer Training Workshop
Traveo™ II Ethernet Mac

Q1 2021

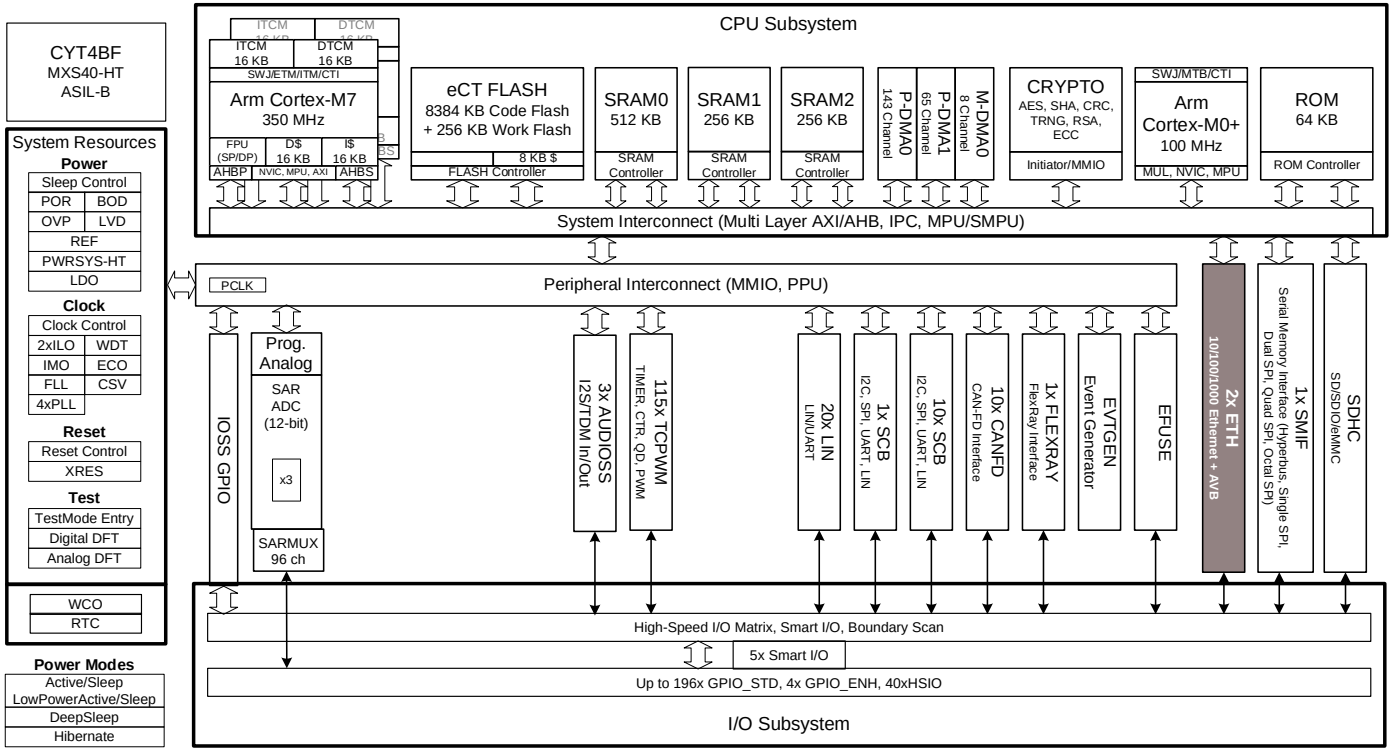
Target Products

› Target product list for this training material

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Body Controller High	CYT3BB/4BB	Up to 4160 KB
Traveo II Automotive Body Controller High	CYT4BF	Up to 8384 KB
Traveo II Automotive Cluster	CYT3DL	Up to 4160 KB
Traveo II Automotive Cluster	CYT4DN	Up to 6336 KB

Introduction to Traveo II Body Controller High

› Ethernet MAC is located in the peripheral blocks

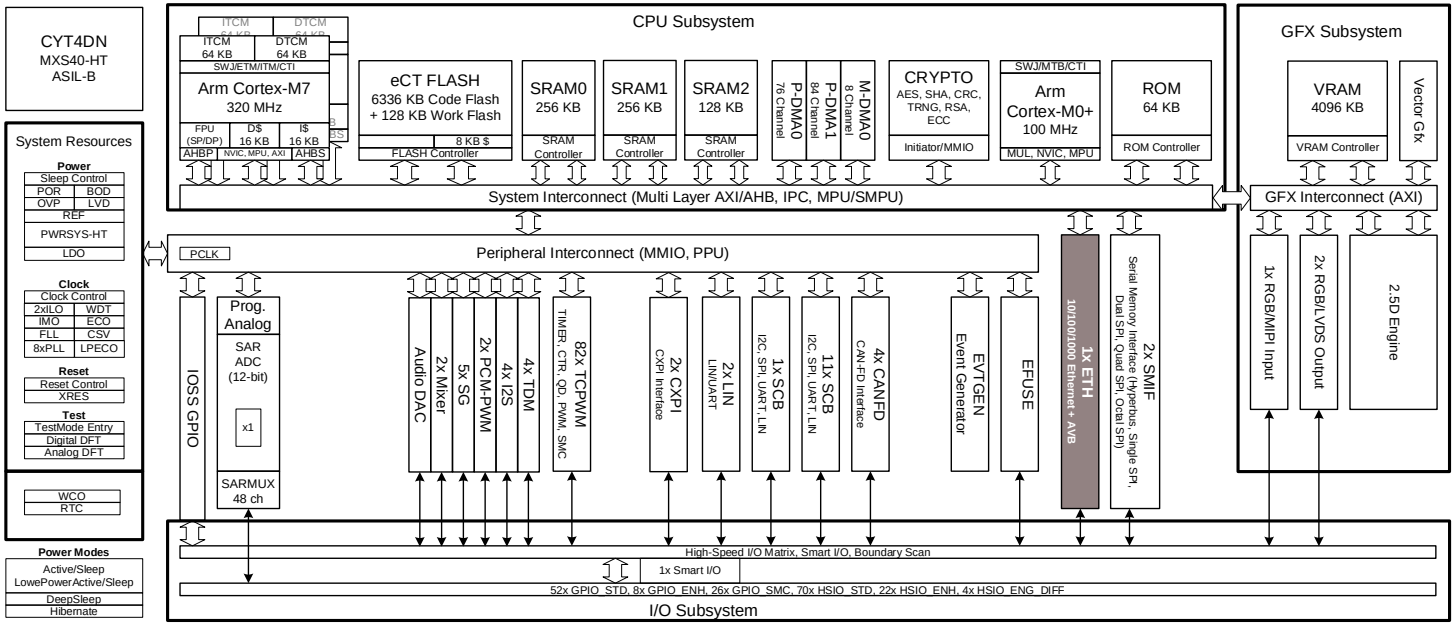


Hint Bar

Review TRM section 31 for additional details

Introduction to Traveo II Cluster

- Ethernet MAC is located in the peripheral blocks

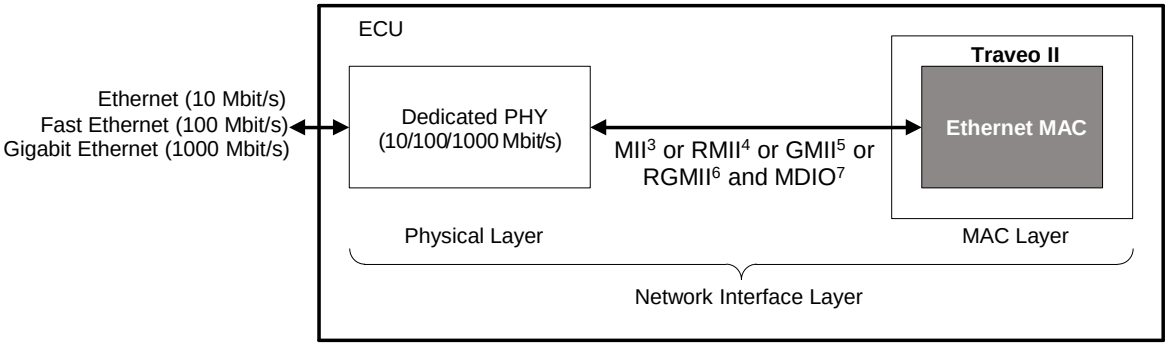


Hint Bar

Review TRM section 31 for additional details

Ethernet MAC Overview

› Ethernet MAC[1] module transmits and receives IEEE 802.3 frames with the PHY[2] device



Hint Bar

Review TRM section 31.1 for additional details

Review the device-specific datasheet to confirm which PHY interfaces are supported in the device

[1] MAC: Media Access Control
[2] PHY: Physical layer
[3] MII: Media Independent Interface
[4] RMII: Reduced Media Independent Interface
RMII is the standard for reducing the number of signals needed to connect the PHY to the MAC compared to MII
[5] GMII: Gigabit Media Independent Interface
[6] RGMII: Reduced Gigabit Media Independent Interface
RGMII is the standard for reducing the number of signals needed to connect the PHY to the MAC compared to GMII
[7] MDIO: Management Data Input/Output

Ethernet MAC Features

- MII, RMII, GMII, and RGMII PHY interface
- MDIO interface for PHY management
- 10/100/1000 Mbps Ethernet MAC compatible with IEEE 802.3
- Full-duplex
- Jumbo frame[1] (Max 1536 bytes)
- IEEE 802.1Q: Virtual LAN (VLAN)
- IEEE 802.3: Pause frame
- IEEE 802.1BA: Audio video bridging systems
- IEEE 802.1Qav: Forwarding and queuing enhancements for time-sensitive streams
- IEEE 802.1AS: Timing and synchronization for time-sensitive applications in bridged LANs
- IEEE 1588 – Precision time protocol

Hint Bar

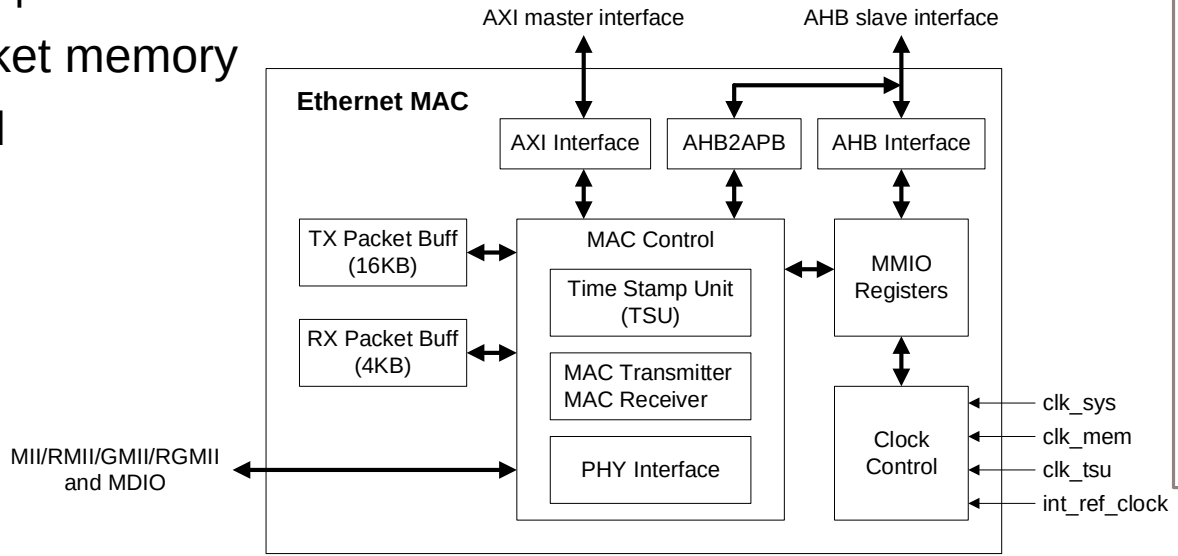
Review TRM section 31.1 for additional details

Review the device-specific datasheet to confirm which PHY interfaces are supported in the device

[1] Jumbo frame is not standardized by IEEE

Ethernet MAC Components

- MAC control
  - PHY interface
  - MAC transmitter/receiver
  - Time stamp unit
- TX/RX packet memory
- CLK control



Hint Bar

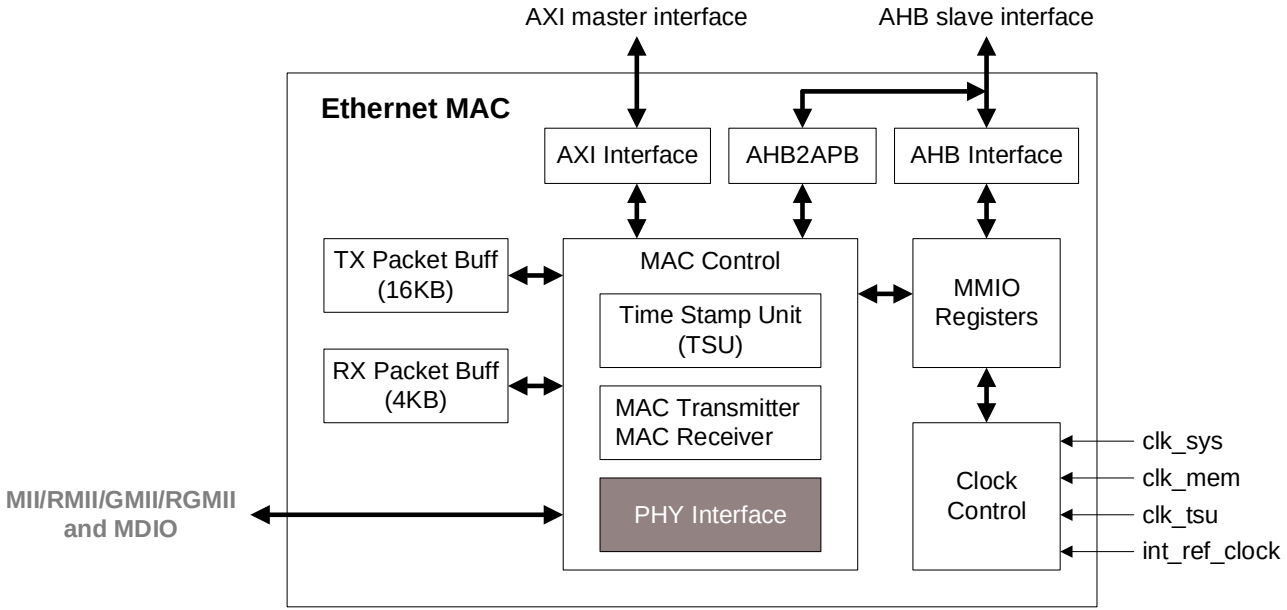
Review TRM section 31.2 for additional details

Refer to the Features List in the datasheet for additional details

Review the device-specific datasheet to confirm which PHY interfaces are supported in the device

PHY Interface

- Supports MII/RMII/GMII/RGMII PHY interface
- Supports MDIO interface



Hint Bar

Review TRM section 31.3.14 for additional details

Review the device-specific datasheet to confirm which PHY interfaces are supported in the device

PHY Interface Types

› Supports the following interface types and transfer rates

Interface Type	Transfer Rate		
	10 Mbps	100 Mbps	1000 Mbps
MII	✓	✓	-
RMII	✓	✓	-
GMII	-	-	✓
RGMII	✓	✓	✓

Hint Bar

Review TRM section 31.3.14 for additional details

Review the device-specific datasheet to confirm which PHY interfaces are supported in the device

MII/RMII/GMII/RGMII Interface

› Supported signals: transmitter/receiver signals

Pin Name	Function of signals	MII	RMII	GMII	RGMII
TXD[1:0]	Transmit data [1:0]	✓	✓	✓	✓
TXD[3:2]	Transmit data [3:2]	✓	-	✓	✓
TXD[7:4]	Transmit data [7:4]	-	-	✓	-
TX_CTL	Transmit enable	✓	✓	✓	✓
TX_ER	Transmit error	✓	-	✓	-
TX_CLK	Transmit clock	✓	✓	✓	✓
RXD[1:0]	Receive data [1:0]	✓	✓	✓	✓
RXD[3:2]	Receive data [3:2]	✓	-	✓	✓
RXD[7:4]	Receive data [7:4]	-	-	✓	-
RX_CTL	Receive data valid	✓	✓	✓	✓
RX_ER	Receive error	✓	✓	✓	-
RX_CLK	Receive clock	✓	-	✓	✓
REF_CLK	Operation clock out	-	✓	✓	✓
	Operation clock in	-	✓	✓	✓

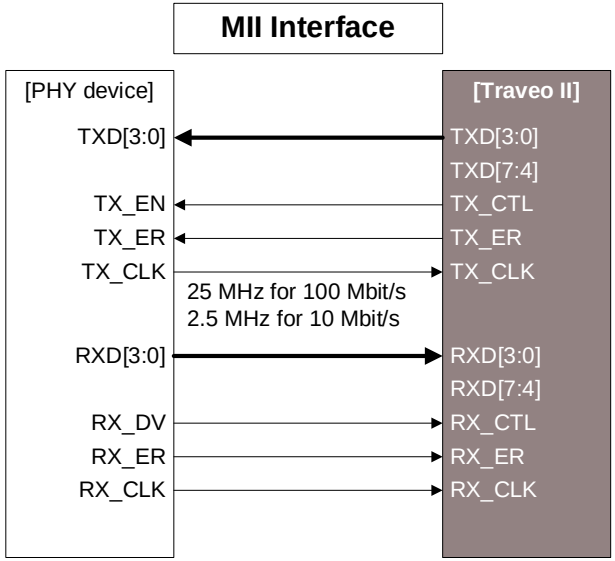
Hint Bar

Review TRM section 31.3.14 and for additional details

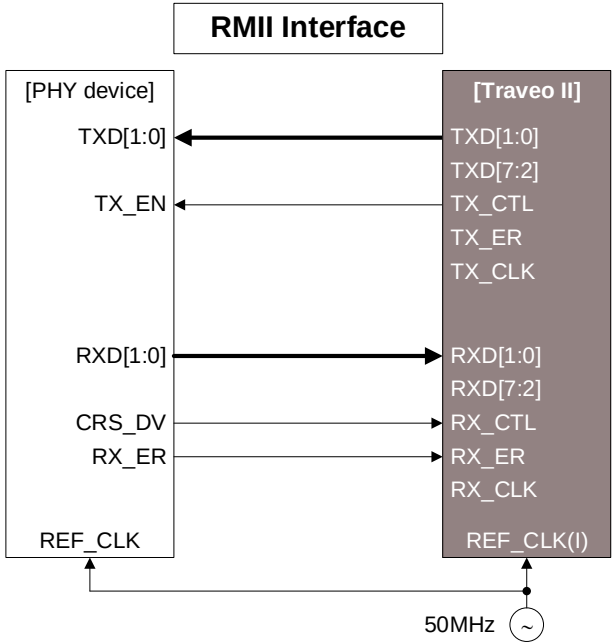
See the Package Pin List and Alternate Functions in the datasheet for additional details

Review the device-specific datasheet to confirm which PHY interfaces are supported in the device

Use Case: MII/RMII Interface



TX and RX clocks are supplied from external PHY



TX and RX clock source can be supplied from either the internal reference clock or the external clock source

ETH_CTRL register must be used to select the reference clock source from the internal reference clock or from HSIO

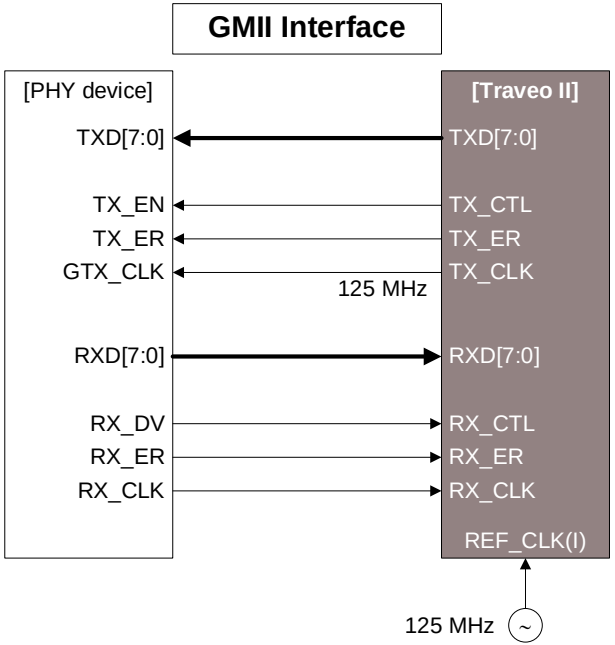
Hint Bar

Review TRM section 31.3.14 for additional details

Review the device-specific datasheet to confirm which PHY interfaces are supported in the device

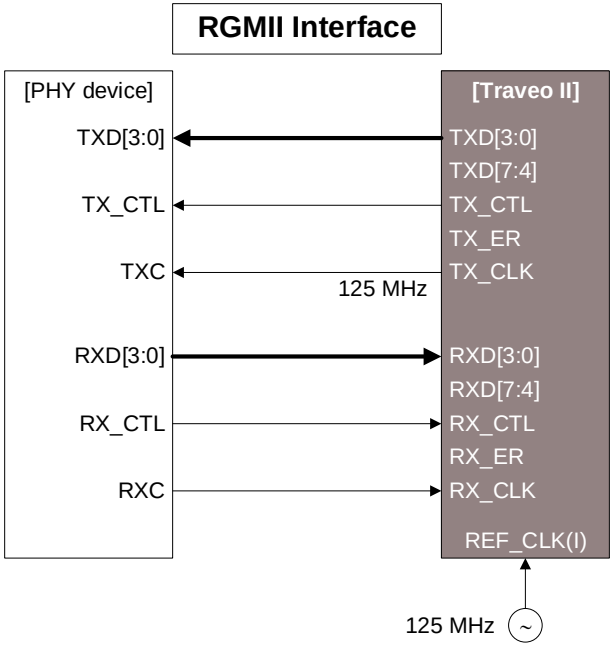
Register info
- ETH_CTRL (REFCLK_SRC_SEL)

Use Case: GMII/RGMII Interface



TX clock source can be selected either from the internal clock source or from HSIO

ETH_CTRL register must be used to select the reference clock source from the internal reference clock or from HSIO



TX clock source can be selected either from the internal clock source or from HSIO

ETH_CTRL register must be used to select the reference clock source from the internal reference clock or from HSIO

Hint Bar

Review TRM section 31.3.14 for additional details

Review the device-specific datasheet to confirm which PHY interfaces are supported in the device

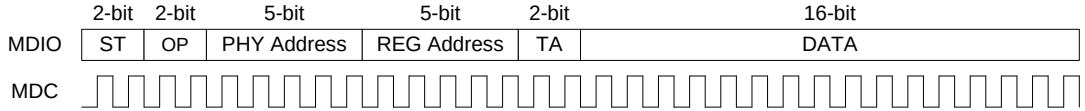
Register info
- ETH_CTRL (REFCLK_SRC_SEL)

MDIO Interface

- Supported signals

Pin Name	Direction	Function of signals
MDIO	I/O	Management Data Input/Output
MDC	O	Management Data Clock

  - MDIO is a single bi-directional tristate signal between Ethernet MAC and PHY
  - MDC is a clock for MDIO
    - MDC is generated by dividing CLK_GR4
    - MDC should not toggle faster than 2.5 MHz (minimum period of 400 ns), as defined by the IEEE 802.3az
- Use case
  - ETH_phy_management register is implemented as a shift register
  - Writing to this register starts a shift operation and outputs to the MDIO pin

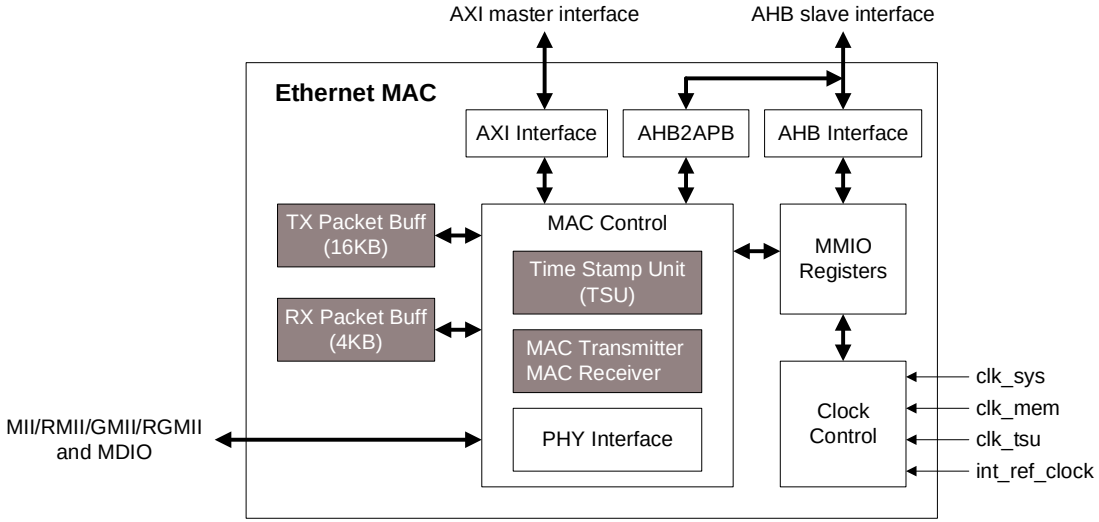


Hint Bar

Review TRM section 31.3.12 for additional details

MAC Transmitter/Receiver, TSU, and Packet Buff

- MAC Transmitter/Receiver and TX/RX Packet Buff
  - Supports transfer of packets between Physical Layer and MAC Layer, and stores data in TX/RX packet buffer
- Time Stamp Unit (TSU)
  - Generates a time stamp for the transmit data and checks the time stamp for the receive data



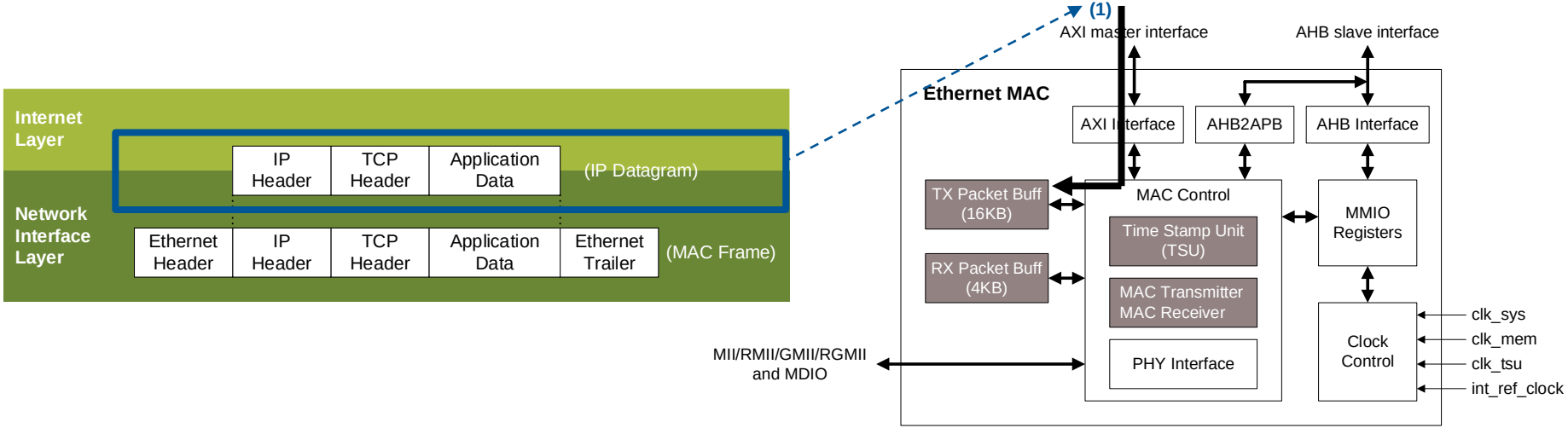
Hint Bar

Review TRM sections 31.3.2 to 31.3.4 for additional details

MAC Transmitter

› Procedure

(1) IP Datagrams are transferred to the TX packet memory via AXI[1]



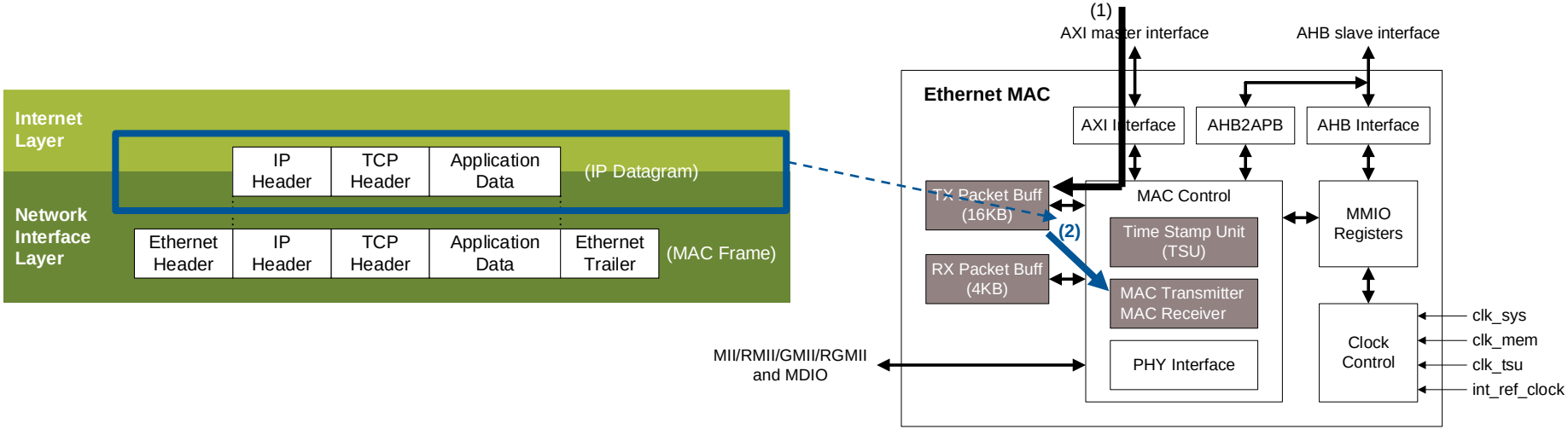
[1] Support to DMA transfer. DMAC is implemented in the MAC Control

MAC Transmitter

Procedure

(1) IP Datagrams are transferred to the TX packet memory via AXI[1]

(2) IP Datagram is transferred to the MAC Transceiver[1]



[1] Support to DMA transfer. DMAC is implemented in the MAC Control.

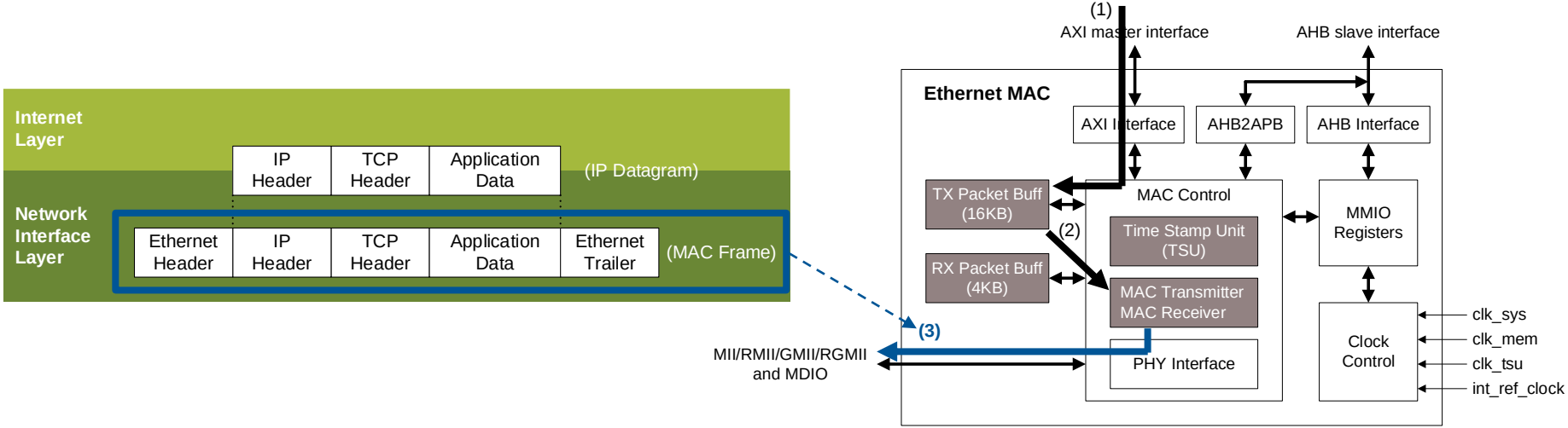
MAC Transmitter

Procedure

(1) IP Datagrams are transferred to the TX packet memory via AXI[1]

(2) IP Datagram is transferred to the MAC Transceiver[1]

(3) MAC frame is multiplexed and transmitted by the hardware

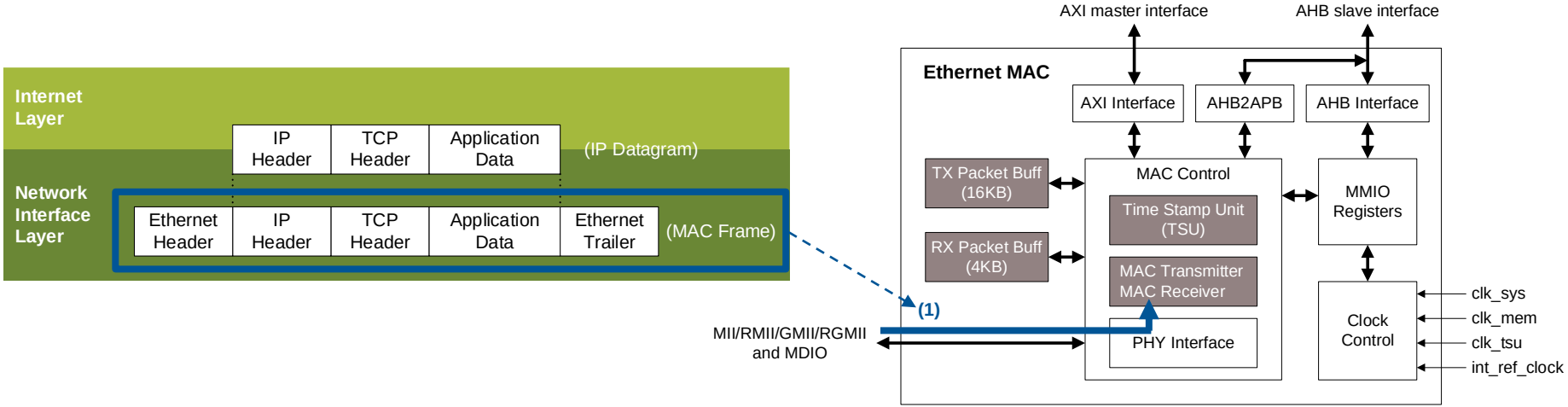


[1] Support to DMA transfer. DMAC is implemented in the MAC Control.

MAC Receiver

Procedure

(1) MAC frame is checked and demultiplexed by the hardware

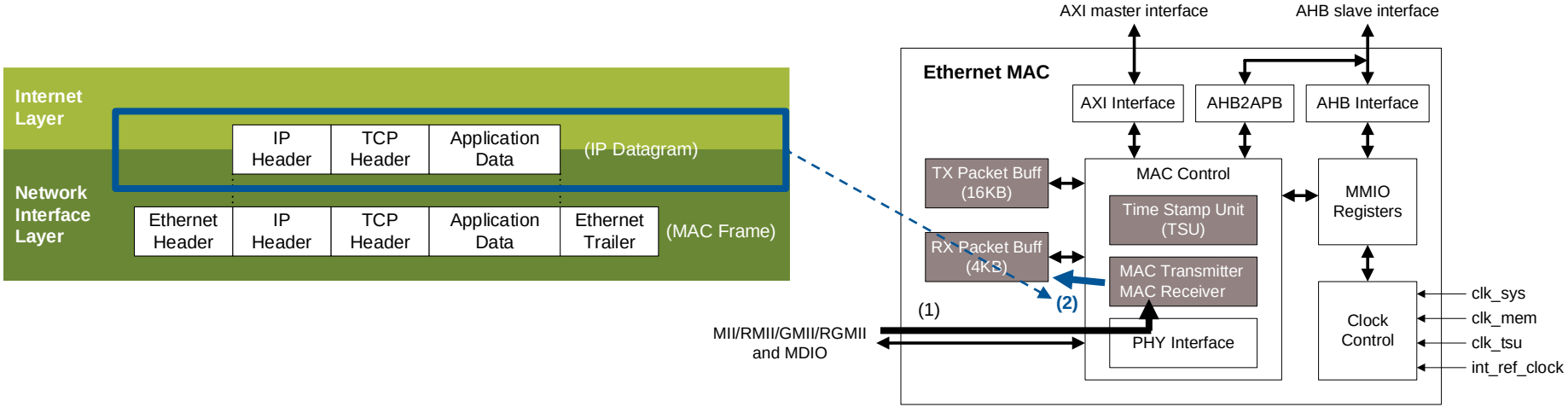


MAC Receiver

Procedure

(1) MAC frame is checked and demultiplexed by the hardware

(2) IP Datagram is transferred to the RX packet memory[1]



[1] Support to DMA transfer. DMAC is implemented in the MAC Control.

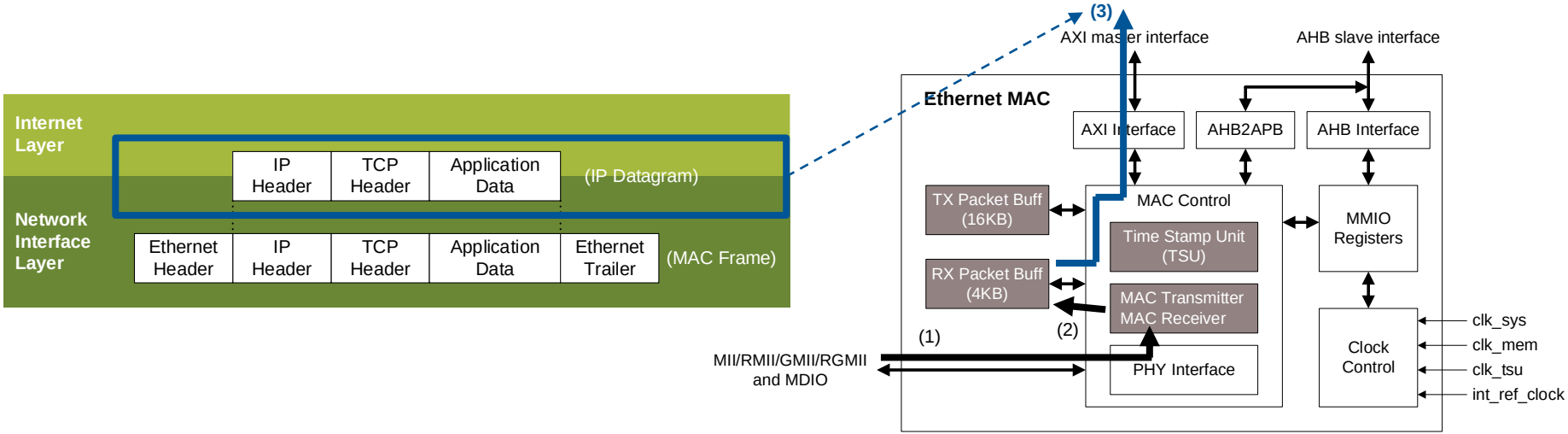
MAC Receiver

Procedure

(1) MAC frame is checked and demultiplexed by the hardware

(2) IP Datagram is transferred to the RX packet memory[1]

(3) IP Datagram is transferred to the internal memory via the AXI bus[1]

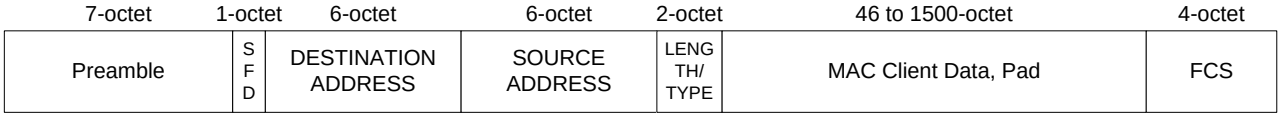


[1] Support to DMA transfer. DMAC is implemented in the MAC Control.

MAC Frame

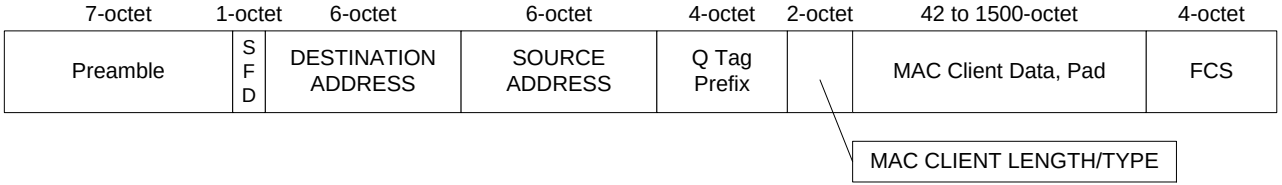
Frame format

Basic Frame



Notes:
SFD: Start of Frame Delimiter
FCS: Flag check sequence

Q-tagged Frame

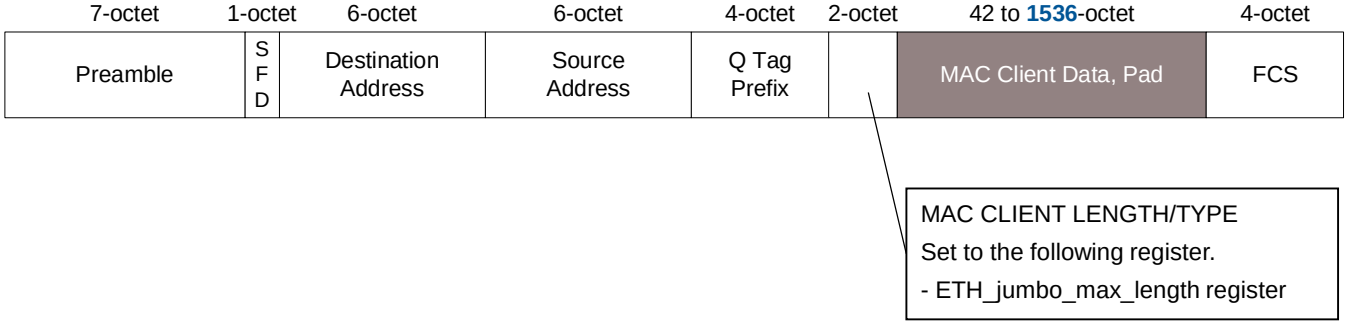


Hint Bar

Review the Register TRM for additional details

Jumbo Frame Support

› The maximum length of the Traveo II jumbo frame payload is 1536 bytes



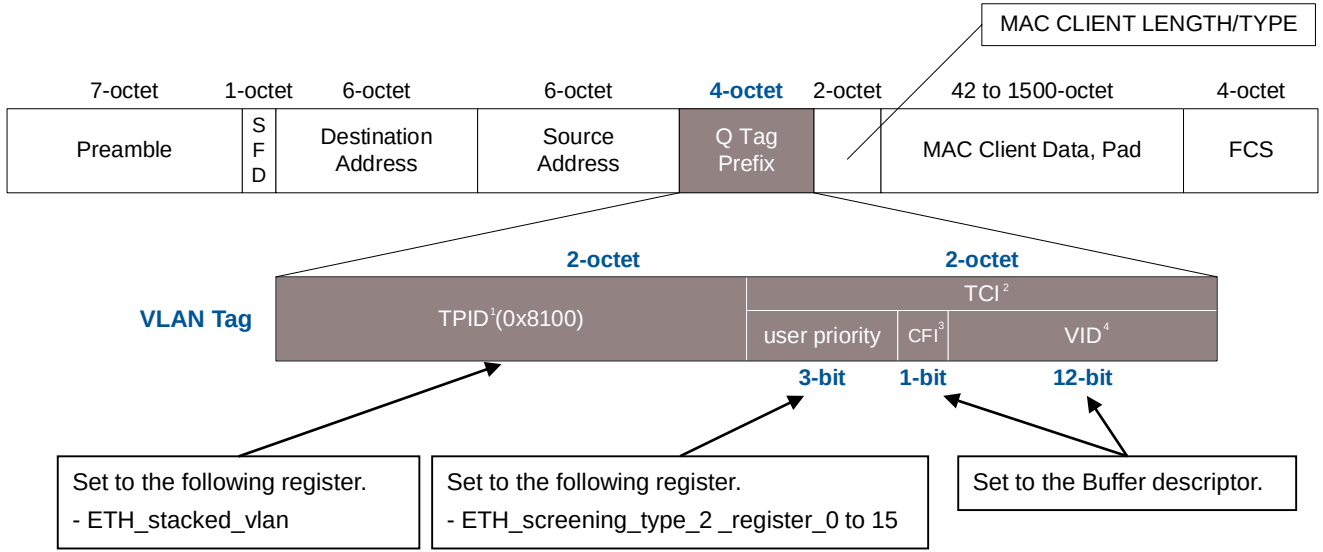
Hint Bar

Review the Register TRM for additional details

Register Info
- ETH_jumbo_max_ length

VLAN Support

- Provides a virtual LAN group in the network by VLAN tag
- VLAN tag is inserted into the Q-tagged frame



Hint Bar

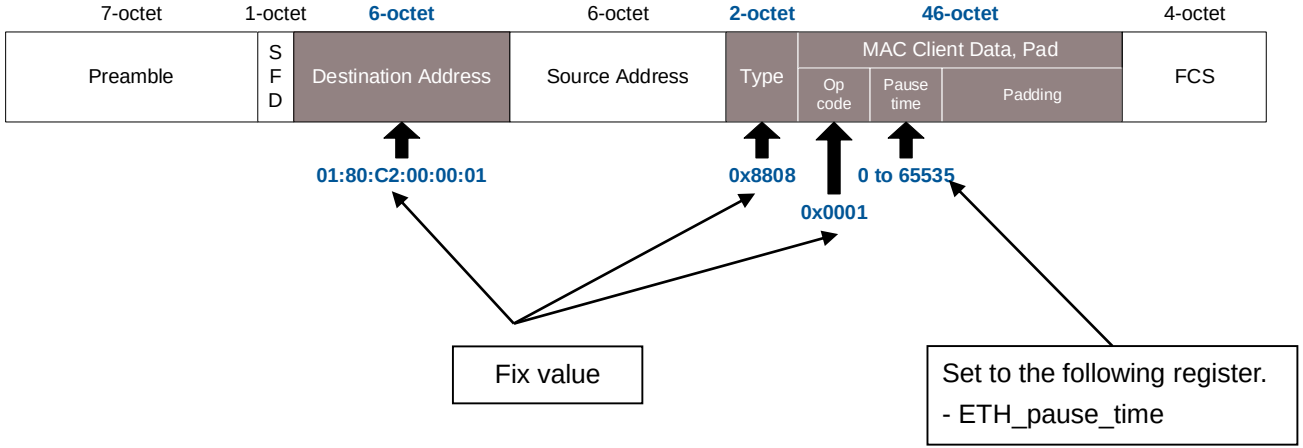
Review the Register TRM for additional details

Register info
- **ETH_network_config**
- **ETH_stacked_vlan**
- **ETH_dma_config**
- **ETH_screening_type_2 _register_0 to 15**

[1] TPID: Tag Protocol Identifier
[2] TCI: Tag Control Information
[3] CFI: Canonical Format Indicator
[4] VID: VLAN identifier

Pause Frame Support

› Pause frame is used to prevent self-buffer overflow



Hint Bar

Review the Register TRM for additional details

Register info
- ETH_network_config
- ETH_pause_time

Audio Video Bridging Systems Support

- Supports the timing and synchronization (IEEE 802.1AS)
- Supports the TSU[1]
  - Ethernet MAC has a TSU compatible to IEEE 1588
- Supports the FQTSS[2] (IEEE 802.1Qav)
  - Ethernet MAC has registers to support FQTSS
  - FQTSS is controlled by software using registers and supports priority control of transmission data

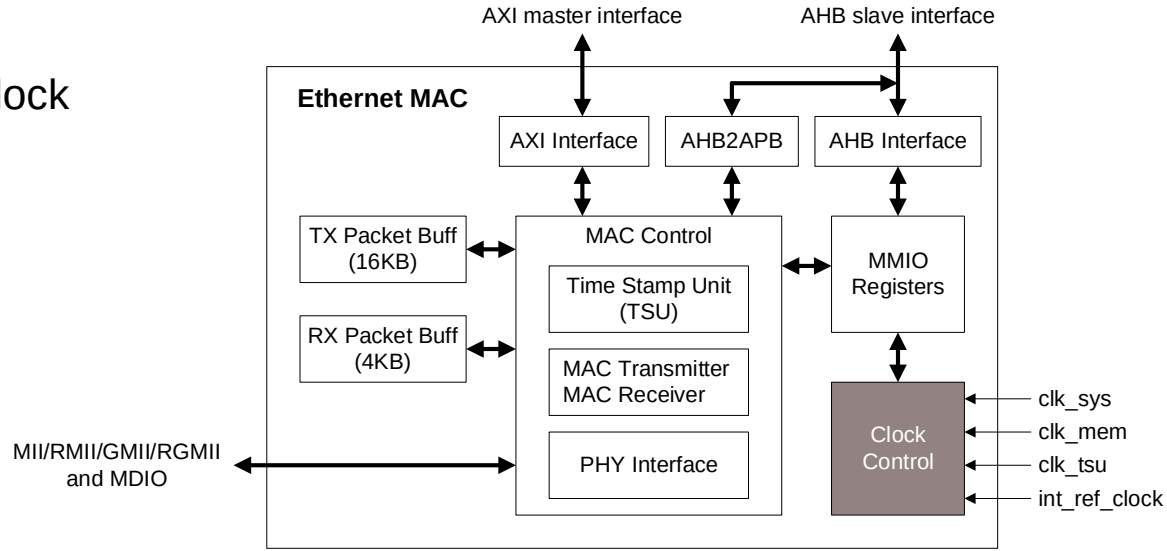
Hint Bar

Review the Register TRM for additional details

[1] TSU: Time Stamp Unit
[2] FQTSS: Forwarding and Queuing Enhancements for Time-Sensitive Streams

Clock Control

- The following clocks are needed to execute the internal operation of Ethernet MAC
  - clk_sys
  - clk_mem
  - clk_tsu
  - int_ref_clock



Hint Bar

Review TRM section 31.3.15 for additional details

Clock Sources

› Usage of each clock is listed here

Clock	Function
clk_sys	To generate MDC clock and for AHB operation clk_sys is derived from CLK_PERI
clk_tsu	TSU clock for TSU timer
clk_mem	Fast clock for AXI operation
int_ref_clock	Internal reference clock supplied from PLL

Hint Bar

Review TRM section 31.3.15 for additional details

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Revision History

Revision	ECN	Submission Date	Description of Change
**	6399212	12/03/2018	Initial release
*A	6678084	09/19/2019	Updated page 2, 3, 5, 6, 8, 11 to 20, 21, 24, 26, 27 Added page 4
*B	6950716	08/17/2020	Updated MII and RMII Interface description on page 11.
*C	7051240	12/22/2021	Updated revision to 0C from 0B Added the new products: page 2 Changed to new block diagram: page 3, 4 Updated TX_CLK assignment: page 10 Updated clock name and description: page 7, 8, 14 to 20, 26, 27 Updated Hint Bar: page 5 to 14, 26, 27
*D	7082784	02/12/2021	Updated page 10 for typo