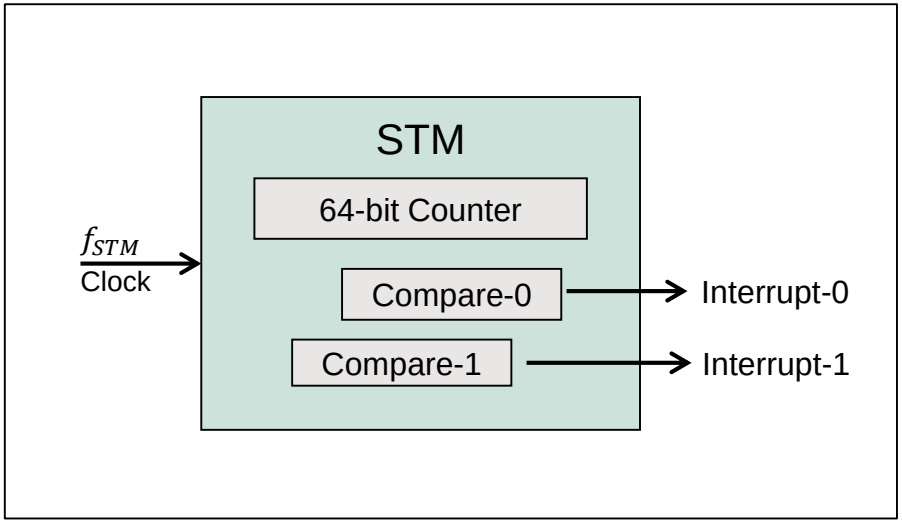
STM

System Timer

AURIX™ TC3xx Microcontroller Training
V1.0 2020-06

STM
System Timer



Highlights

- The System Timer STM is used to generate a time base e.g. for an OS, as well as to generate trigger events
- There are as many STM modules as there are CPUs in the system. Thus each CPU can use one STM for its time base

Key Features

Free-running 64-bit counter

Flexible interrupt service request generation

Customer Benefits

- Fits perfectly the generation of OS time base and triggering events
- Indication of events with assigned priority for highest flexibility

STM
Free-running 64-bit counter

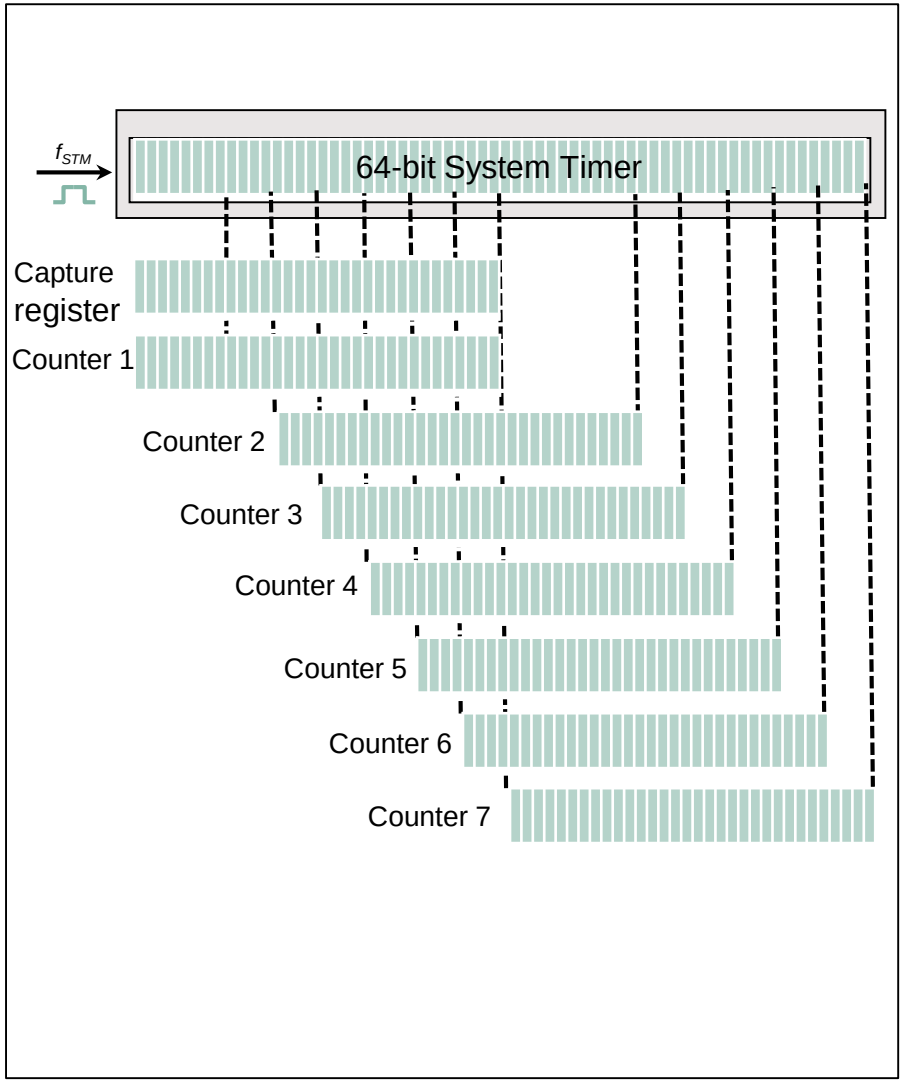
The STM has a 64-bit counter which is clocked by f_{STM} from the CCU (Clock Control Unit).

The system timer value can be read via 7 registers, each selecting a 32-bit range of the system timer value.

Each of these can be used as counters with different resolution and range.

Due to the 64-bit width, the entire counter needs to be read with two load instructions. The timer will continue counting between the load operations, therefore there is a chance that the read values will not match. In order to enable synchronous and consistent reading of the STM content, a capture register was implemented.

This capture register holds the upper value of the timer why the lower part is read. Therefore the second load operation will read the content of the capture register.



STM
Flexible interrupt service request generation

The STM counter can be compared against the values in two comparison registers.

If the values match, a compare match event is generated from either of the comparisons.

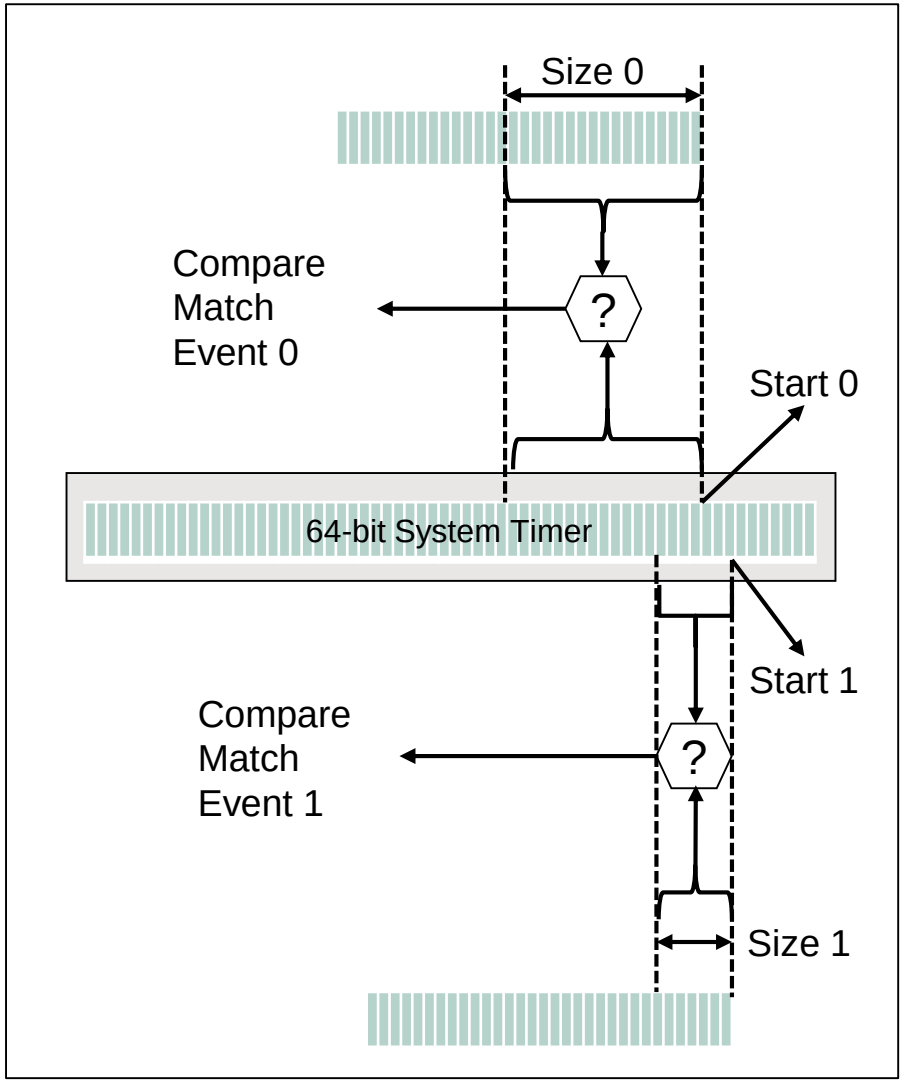
Two parameters are programmable for the compare operations:

- START: First bit (LSB) location to be taken for the compare operation.
- SIZE: Number of bits to be compared (starting from zero).

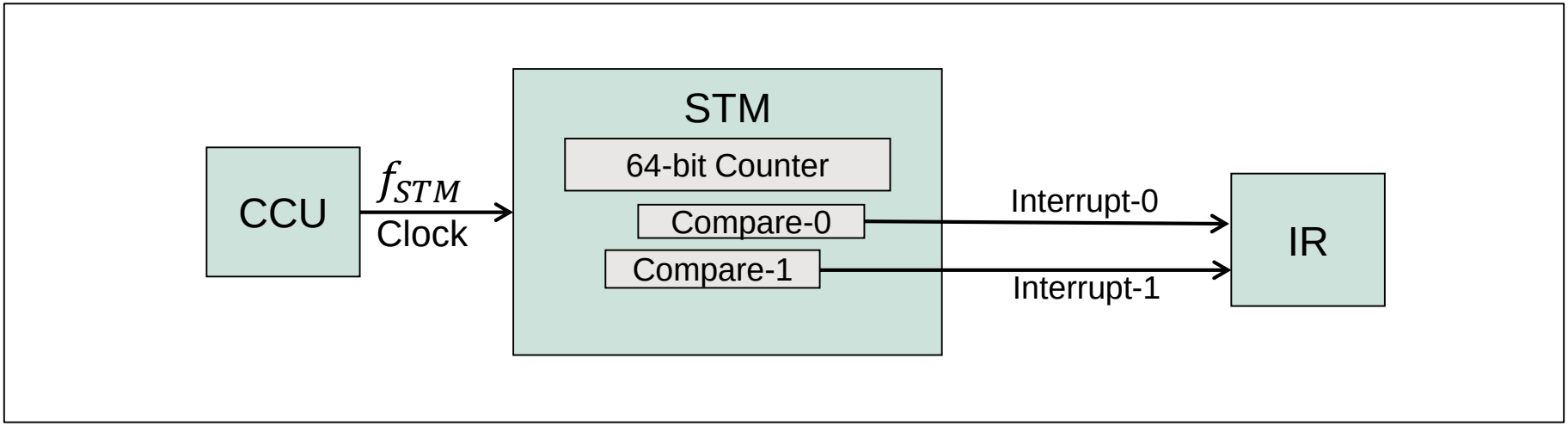
Using the START and SIZE configuration, it is even possible to check for single bit transitions (setting the size to 0 and the start to the bit of interest.

In the right side figure – the following parameters are assumed to be configured:

- SIZE0 = 17; START0 = 10
- SIZE1 = 7; START1 = 7

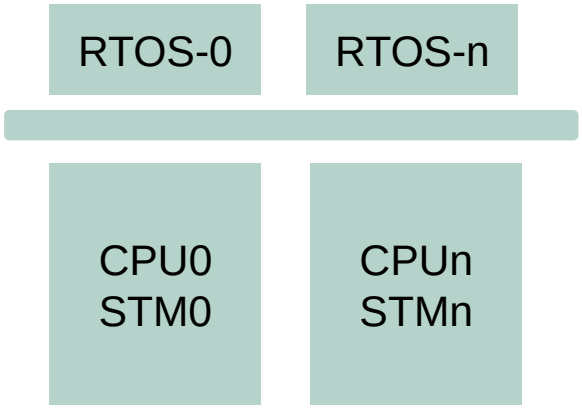


STM
System integration



- Clock to the STM (f_{STM}) is generated from the CCU
  - This is generated from the system PLL after it is enabled
  - The clock divider should be configured in both modules: CCU and STM
- It must be ensured that the f_{STM} is on an integer to the System Peripheral Bus (SPB) clock (f_{SPB})
  - If the integer ratio is not ensured, then the counter value can be wrong

Application example
Operating system time base generation



Overview

STM can be used to generate the time base for a Real-Time Operating System (RTOS), for example as a base for the scheduler.

Advantages

- Different rates of timer interrupt can be configured
- In a multicore system, each CPU can have its own time base

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Do you have a question about this document?
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