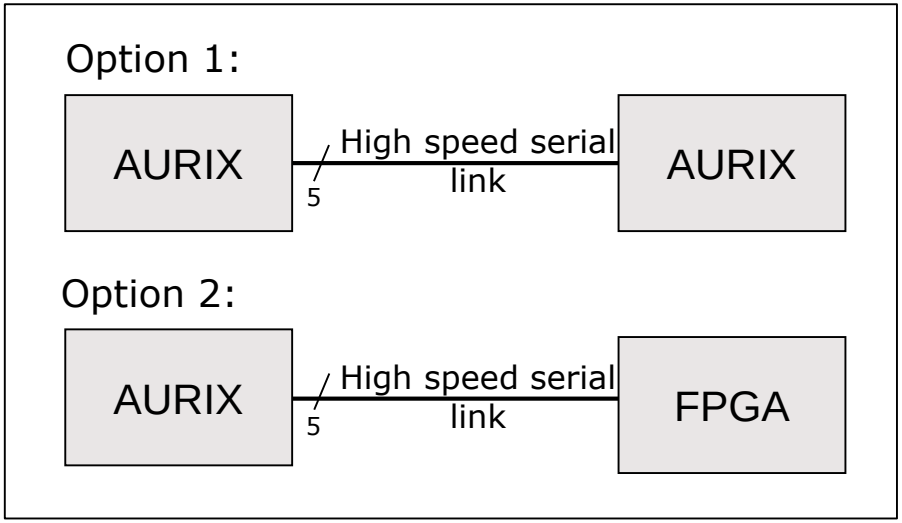
HSSL

High Speed Serial Link

AURIX™ TC2xx Microcontroller Training
V1.0 2019-03

HSSL
High speed Serial Link



Highlights

- High speed communication with up to 320 MBaud between two AURIX devices
- Protocol supported by FPGAs
- Low pin count (2 x 2 LVDS, 1 x clock)
- Triggering of interrupts from remote

Key Features

Act as internal bus master interface

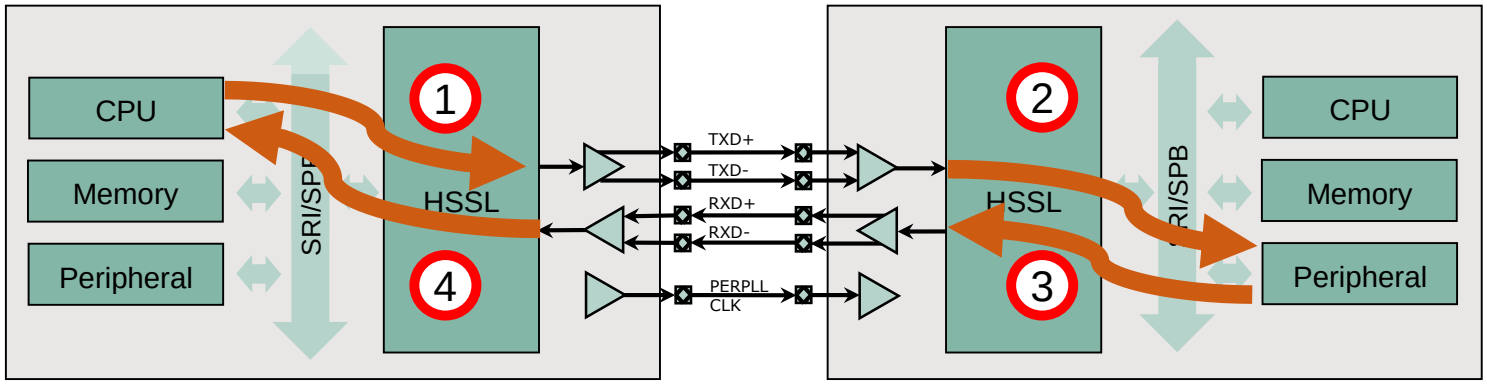
Streaming supported by direct memory access

Access windows for protection and security

Customer Benefits

- Direct access to all registers and memories on remote device. Remote CPU not involved
- Off load CPUs on both devices even for high data bandwidth and short latency use cases
- Avoids possible security impact of powerful communication options given by this module

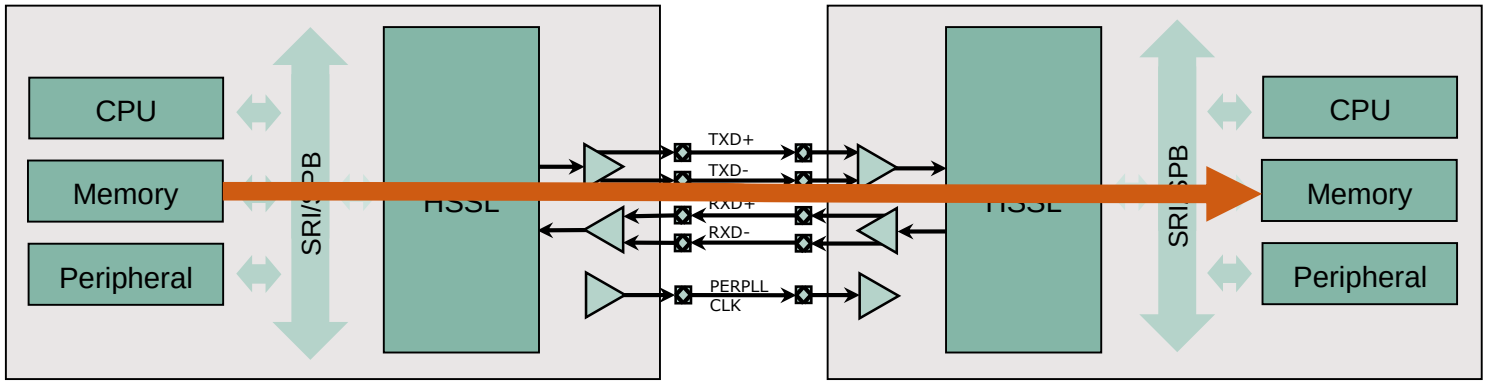
HSSL
Act as internal bus master interface



- Typically CPUx can access local memories and peripheral registers by its master bus interface on the internal local bus
- With HSSL, CPUx can also access remote memories and peripheral registers. For this purpose, on the remote device HSSL module is acting as a bus master – same as the local CPUs can do
- Remote CPUx are not involved in this process
- All accesses to remote peripherals and memories are based on simple and lightweight register accesses to the local HSSL module
- Available protocol frames for this purpose are: 8/16/32bit READ, 8/16/32bit WRITE
- All frames are end-to-end protected by CRC

→ **HSSL makes device boundaries become meaningless and enables you, to focus the combined processing power of the interconnected devices (CPUs and peripherals) for one mission**

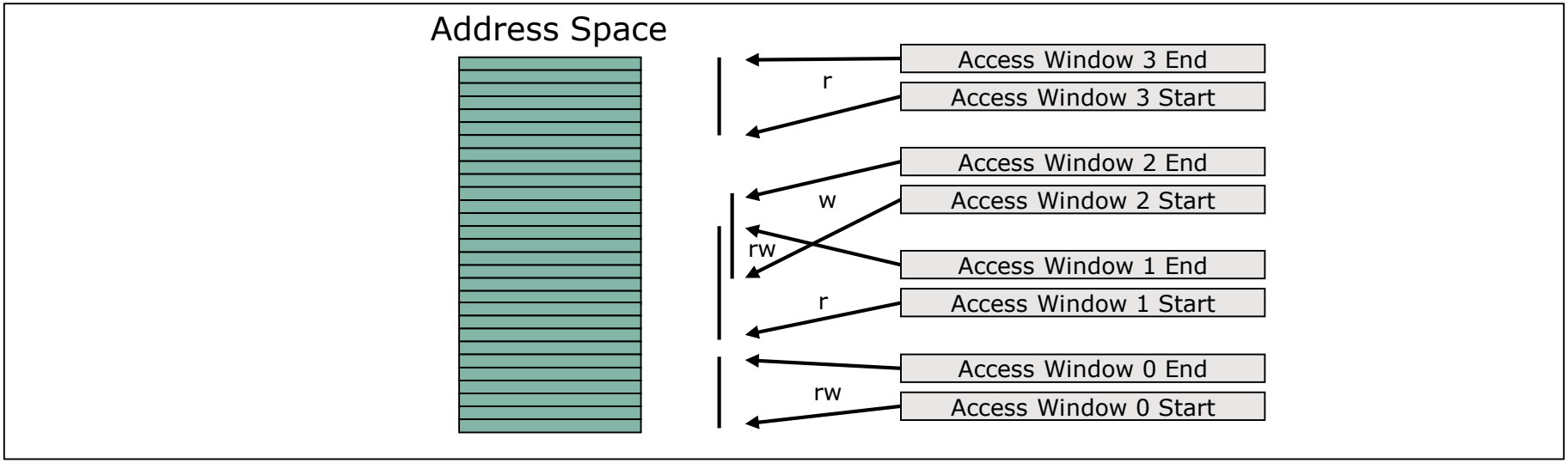
HSSL
Streaming supported by direct memory access



- HSSL has an integrated DMA to autonomously execute data streaming from any memory location of the local device to any memory location on the remote device
- Easy and lightweight streaming setup by CPUx providing source address, destination address and amount of data
- Any CPU can setup streaming also from remote by using HSSL 32bit READ/WRITE accesses
- Support of continuous streaming including double buffering. Once continuous streaming is started, no further CPU interaction is needed to keep streaming alive
- All streaming frames are end-to-end protected by CRC32

→ **High data throughput of up to 84% net bandwidth of 320MBaud uni-directional and 62% net bandwidth bi-directional**

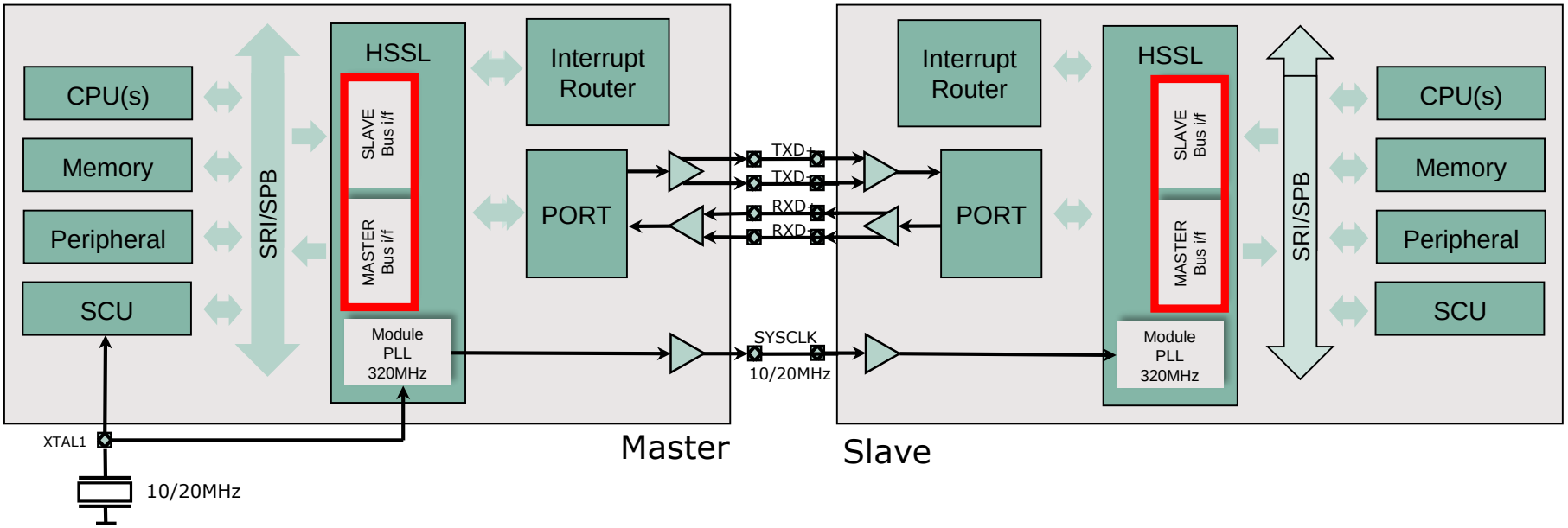
HSSL
Access windows for protection and security



- HSSL allows remote devices to access the entire address and register space of the local device. Depending on the application, this could result in security risks. To eliminate these risks, access windows are implemented inside hardware
- Four independent access windows can be defined granting RW, W or R access. Every read/write request not passing any of the access windows is rejected by hardware
- After reset, by default, the complete address space is protected for read and write
- The registers to setup access windows are at any time protected from being accessed from remote

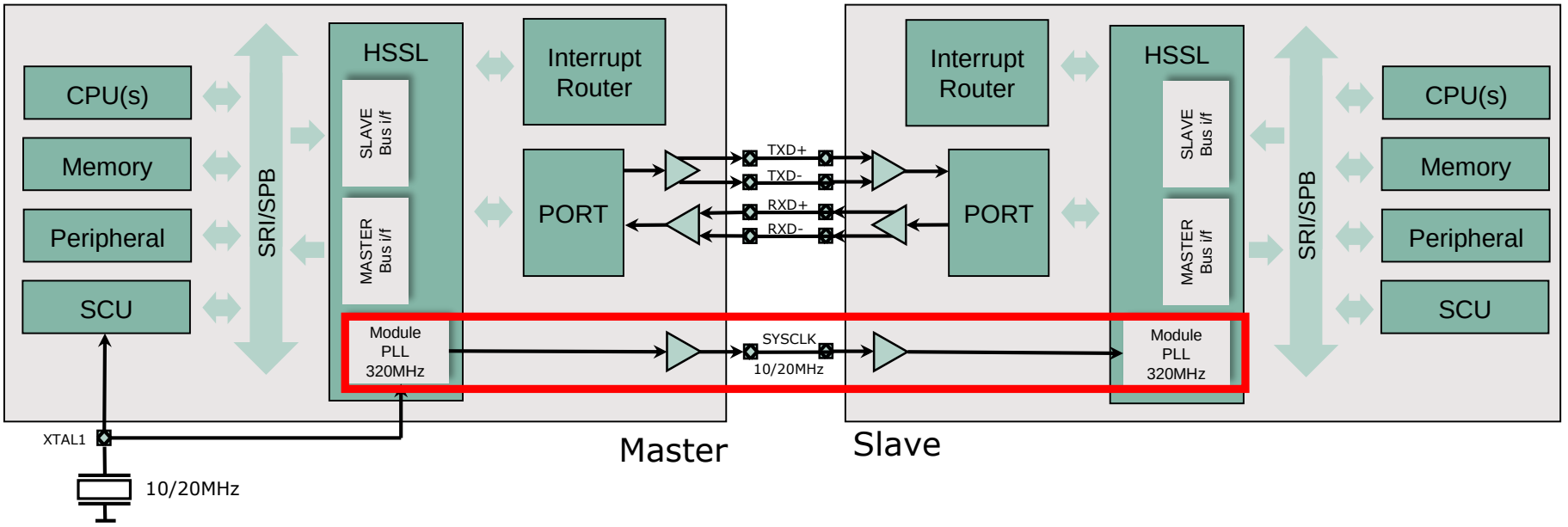
  → **Device is at any time in full control which registers or memory can be accessed from remote**

HSSL
System integration



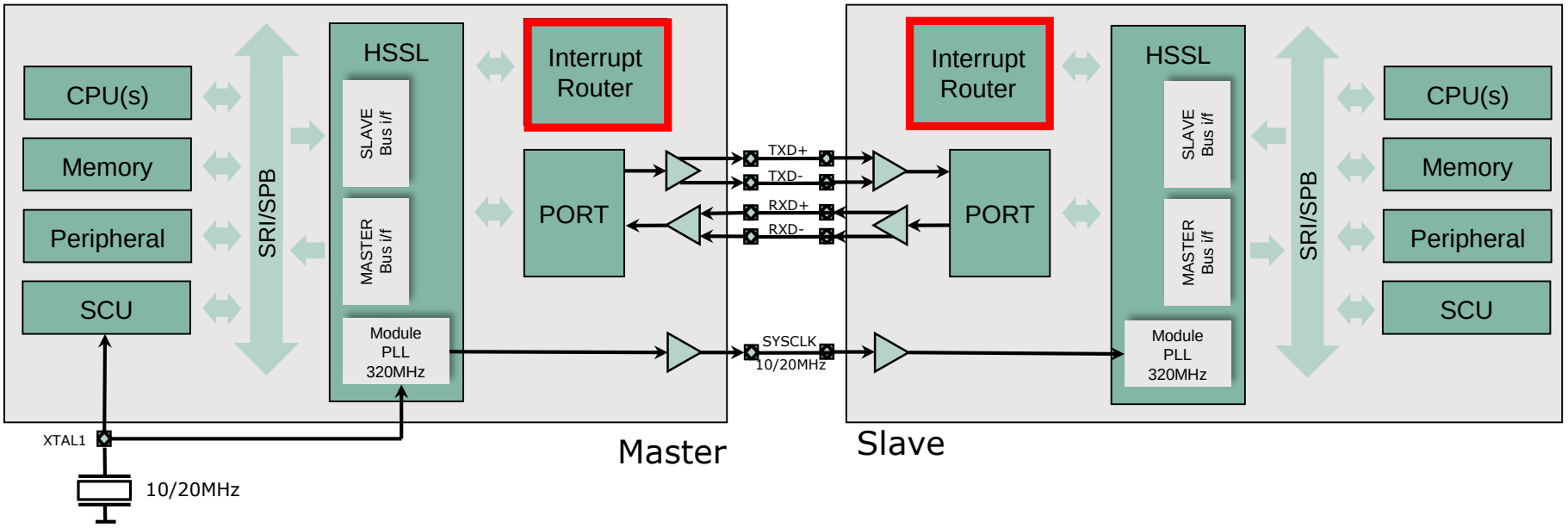
- HSSL has slave and master access on the internal bus
- **Slave interface is used** by bus masters (like CPU or HSSL module itself) to access the HSSL registers for configuration and to initiate communication transactions
- **Master interface is used** by the HSSL module to
  1. read/write memories and registers during execution of transactions
  2. read pre-programmed linked linked lists (e.g. prepared by CPUx) from memory to execute autonomously a sequence of transactions

HSSL
System integration



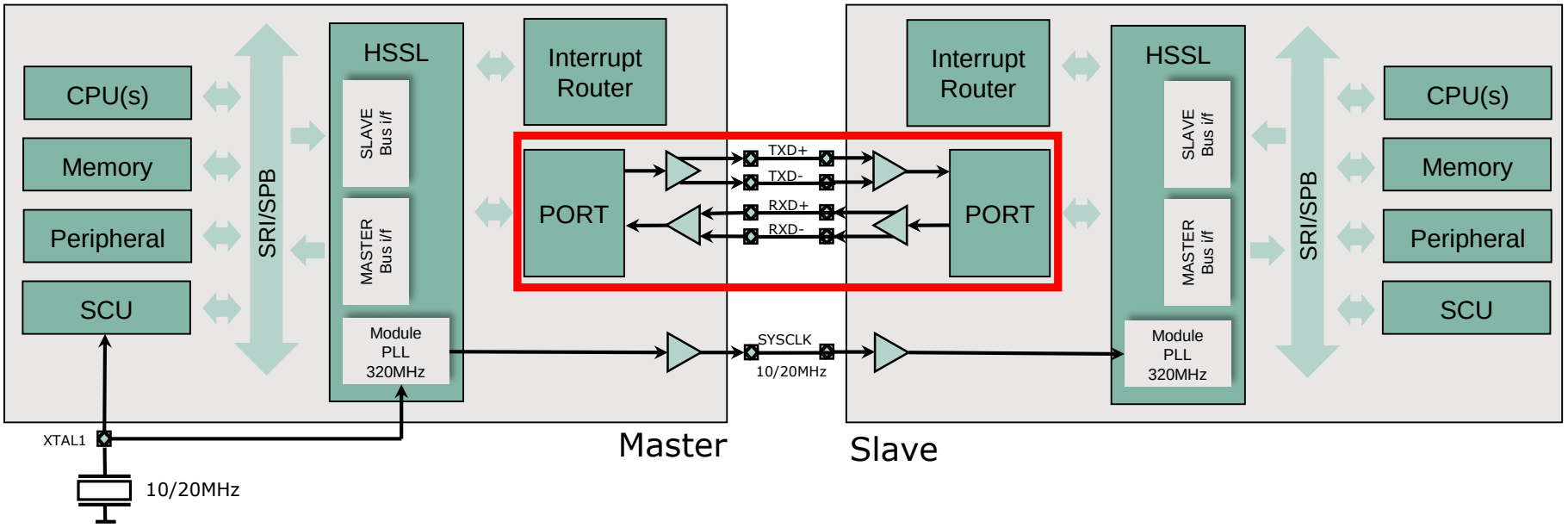
- On physical layer, HSSL integrates an independent PLL to generate the 320MHz PHY clk. Typically on master device the input clock of the HSSL module PLL is derived from oscillator crystal
- On physical layer the two interconnected devices have an asymmetric setup: Master device is providing its clock to the slave device for frequency matching
- On protocol layer the asymmetric master/slave setup of physical layer is not visible. Here both devices behave symmetric and all communication options are equally available to both devices

HSSL
System integration



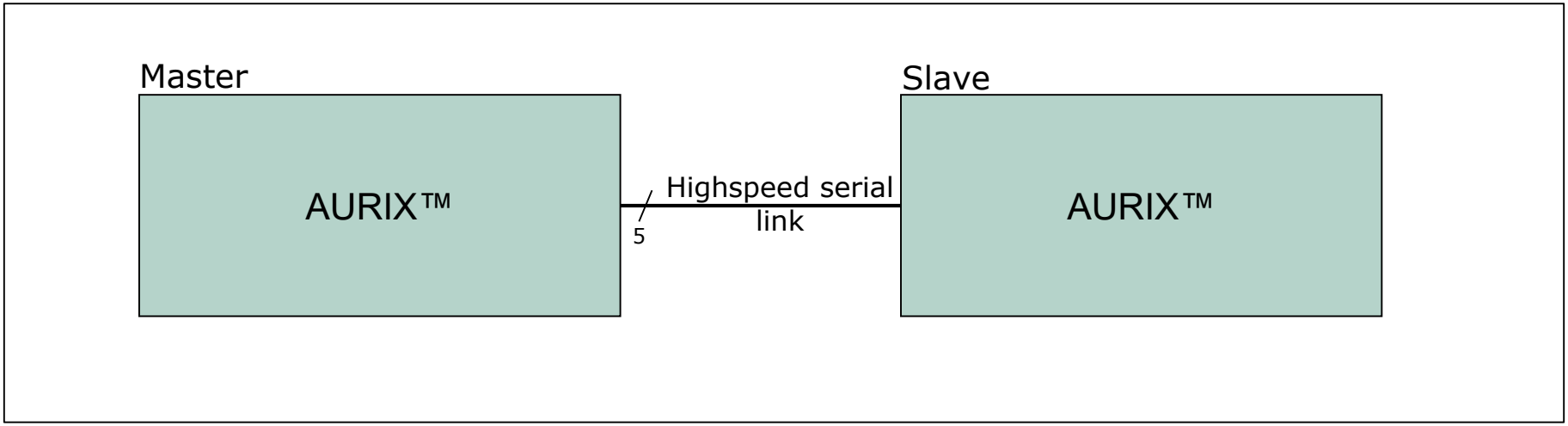
- HSSL module provides its interrupts to interrupt router for further distribution (to DMA and CPUx) and priorization
- Interrupts provided by HSSL are used to monitor the communication and status of the module
- On top, to trigger interrupts from remote, HSSL module provides four functional TRIGGER-interrupts
- TRIGGER-interrupts are mostly used for short latency notifications to CPUx, typically for remote function calls implemented inside software

HSSL
System integration



- HSSL uses four port pins for low voltage differential signaling. One LVDS-pair is used as output and one LVDS-pair is used as input
- Terminal resistors are integrated into the pads and can be optionally enabled

Application example
Integrate resources of two AURIX™ into one system



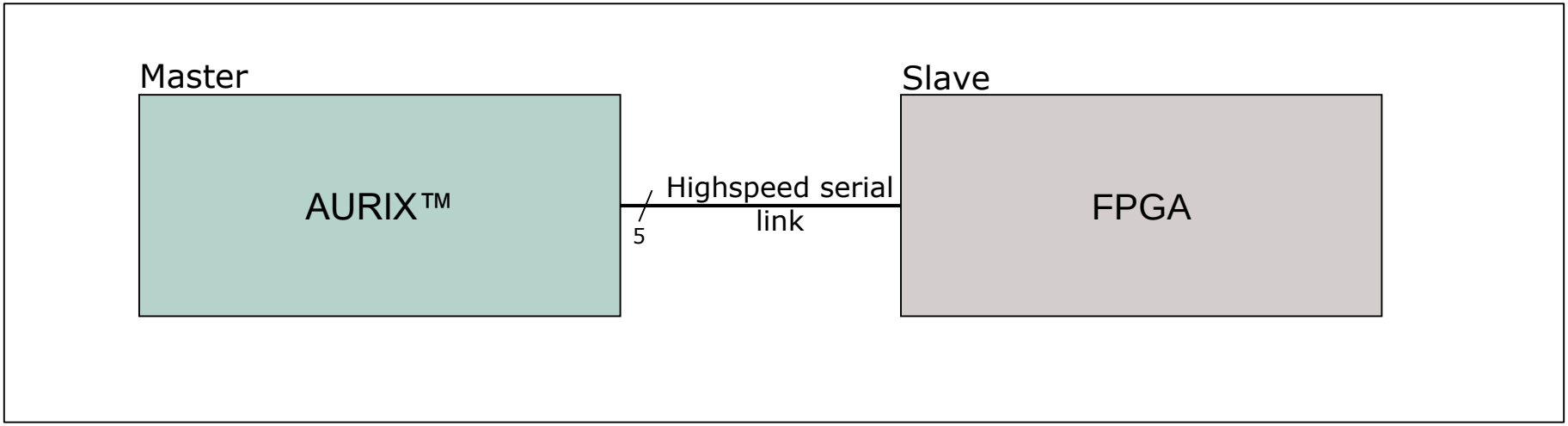
Overview

- Smoothly integrate two AURIX™ into one system, allowing both devices to have full control and flexibility in controlling the resources of each other

Advantages

- Enable safety applications with upscaled performance and functional extension, if the resources given by only one AURIX™ device do not meet the system requirements
- Use technologies like remote function calls, remote register access and short latency synchronization between two AURIX™

Application example
Integrate AURIX™ and FPGA into one system



Overview

- Smoothly integrate AURIX™ and FPGA into one system, allowing both systems to have full control and flexibility in controlling the resources of each other

Advantages

- Extend functional safety applications up to ASIL-D level provided by AURIX™ with the flexibility and feature set brought to the table by FPGA
- Use technologies like remote function calls, remote register access and short latency synchronization between FPGA and AURIX™

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